Cankaya University Electronics and Communication Engineering Department
ECE 329 Digital Design II Course Outline

Instructor: Orhan Gazi
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Course info: CMOS Families, TTL Families, Asynchronous Sequential Logic, Basic Computer Organization and Design, Central Processing Unit, Computer Arithmetic, I/O Organization, Memory Organization, Pipeline and Vector Organization. VHDL programming


Topics to be covered during the semester:

1. Flip-Flops and memory units.
2. Asynchronous Sequential Logic.
3. Basic Computer Organization and Design
4. Central Processing Unit, Computer Arithmetic
5. I/O Organization
6. CMOS families
7. TTL families
8. Verilog-VHDL programming

Laboratory:

Every week lab sheets will be put in Caglar Arpali’s web-page. Please get a copy of the sheet and do the preparation part at home. Please come to the lab having completed the preparation part, otherwise you may not be allowed to enter to the lab. Assistant will guide you during the lab.

Homework:

I will put homework in my web page. Please do the homework and submit it to the assistants. The necessary information about the homework will be given in the page (deadline, explanation e.t.c)

Grading Policy:

Overall Mark = Midterm % 30 + Final % 40 + HW % 5+ Lab % 20 + Attendance %5

Lab Assistant: Serap ALTAY, Caglar ARPALI